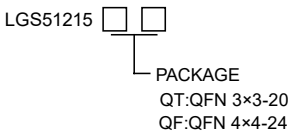
Synchronous Buck Controller with 2-Bit VID Inputs to Select Output Voltages

Check for Samples: LGS51215

Features

- Wide Input Voltage Range: 4.5V-24V
- Selectable Fixed Frequency 300K/400K/600KHz
- 2-Bit VID Control, Programmable Output Voltage and 0V Output can be Configured
- ±1% System accuracy
- Differential Signal Sampling CSN-CSP
- Configurable Output Voltage Switching Rate
- Output Voltage Indication: Power good Function
- Configurable Load Line Compensation Function
- Fast Loop Dynamic Response
- Internal Power Tube Driven Dead Time Control
- Junction Temperature Range From -40℃ to +125℃

Ordering Information



Part	Package	Top Mark
LGS51215QT	QFN 3×3-20	LGS51215YW
LGS51215QF	QFN 4×4-24	LGS51215YW
Y: year code W: week code		

Description

LGS51215 is a DC-DC synchronous buck controller with adjustable output. LGS51215 has a wide input voltage range of 4.5V to 24V. The output voltage can be dynamically switched by the VID0 and VID1 logic signals. The voltage switching rate can be configured by the soft-start Capacitor. FB voltage is configured by a resistor divider network. LGS51215 adopts the current detection control mode, which reduces the complexity of the compensation network. At the same time, it has an ultra-fast loop response speed. The inductor current sampling mode is used. Provides a cycle-by-cycle current limiting function with a maximum load of 30A.

Additional features include: soft-start, soft-stop, thermal shutdown, UVLO undervoltage lockout, gate driver undervoltage lockout, and smart current limit shutdown **timer.**

Applications

- Notebooks, Desktops & Servers
- I/O Supplies
- Power Bus
- Low-power CPU/GPU power rail

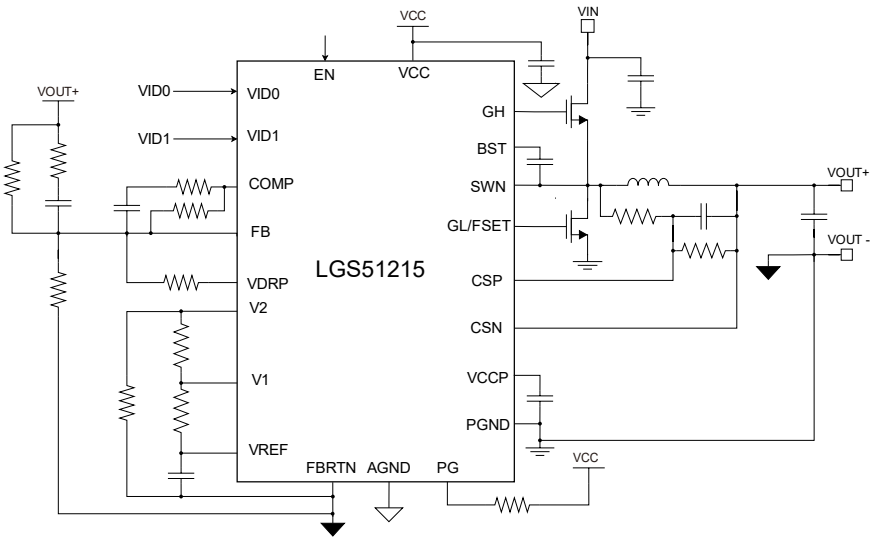


Figure 1.1 Typical Application

Revision History

Note: Page numbers in previous editions may differ from current edition page numbers.

Changes from RevA V0.1 Dec.2021 to V0.2 Jan.2022	Page
Updated internal logic diagram and package information	ALL
Changes from RevA V0.2 Jan.2022 to V0.3 Feb.2022	**Page**
Updated some data and descriptions	ALL
Changes from RevA V0.3 Feb.2022 to V0.4 Mar.2022	**Page**
Updated some data and descriptions	ALL
Changes from RevA V0.4 Mar.2022 to V1.0 May.2022	**Page**
Updated some data and descriptions	ALL

- The current document is the revised version RevA V1.0, and the relevant parameters of this manual are only recognized for the relevant indicators and descriptions of this version.

Package and Pinout Diagram

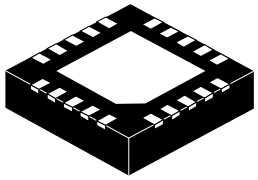


Figure 3.1 QFN3X3-20L Package

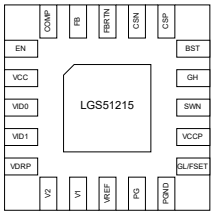


Figure 3.2 Package Reference Top View

Pin Function

Table 4.1 Pin Function Description

Pin	Name	Description
1	EN	Logic control for enabling the switcher. High level enables the output; Low level disable.
2	VCC	Analog control power input. Externally connect at least 2μF ceramic capacitor.
3	VID0	Output voltage programming control. Controls output voltage simultaneously with VID1.
4	VID1	Output voltage programming control. Controls output voltage simultaneously with VID0.
5	VDRP (1)	Load line compensation. Putting a suitable resistor between VDRP and FB pin can compensate the output line loss.
6	V2	Feedback voltage programming. The output voltage can be configured by connecting an appropriate resistor divider in series between VREF, V1, and V2.
7	V1	Feedback voltage programming. The output voltage can be configured by connecting an appropriate resistor divider in series between VREF, V1, and V2.
8	VREF	reference signal. Configure the output voltage together with V1 and V2, externally connect a ceramic capacitor of no less than 2nF, configure the output voltage soft-start time and output voltage switching rate.
9	PG	Power good indicator of the output voltage. Open−drain output.
10	PGND	Ground reference and high−current return path for the bottom gate driver.
11	GL/FSET	Gate driver output of bottom N−channel MOSFET. And it is also used to set up switching frequency by connecting a resistor from this pin to ground.
12	VCCP	Power supply for MOSFET gate drive
13	SWN	Switch node between the top MOSFET and bottom MOSFET.
14	GH	Gate driver output of the top N−channel MOSFET.
15	BST	Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin.
16	CSP	Inductor current differential sense non−inverting input.
17	CSN	Inductor current differential sense inverting input. It also discharges VOUT during soft-stop.
18	FBRTN	Feedback Return Input/Output. This pin remotely senses the output voltage.
19	FB	Output voltage feedback.
20	COMP	Output of the error amplifier.
21	AGND	Analog ground. Bottom thermal pad.

(1) If this function is not needed, please keep this pin empty.

Absolute Maximum Ratings (1)

Table 5.1

Parameters	MIN	MAX	UNIT
VCC to GND	-0.3	6	V
SWN to GND	-5	28	
BST to SWN、BST to GH、VCCP to PGND	-0.3	6	
BST to GND	-0.3	34	
FBRTN、PGND to AGND	-0.3	+0.3	
GL to PGND	-0.3	MIN(VCCP+0.3,6)	
GH to SWN	-0.3	BST+0.3	
Other Pin to GND	-0.3	6	
Storage temperature（T_{stg}）	- 65	+ 150	℃
Junction Temperature（T_J）	- 40	+ 125	

(1) Temperature range: -40°C - +125°C (unless otherwise specified), if the device operating conditions exceed the above "absolute maximum", it may cause permanent damage to the device. This is only the limit parameter, it is not recommended to operate the device under the limit value or beyond the limit value, the device working under the limit condition for a long time may affect its reliability.

Handling Ratings

Table 6.1

			VALUE	UNIT
V_{ESD}	Electrostatic discharge test	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±1000	V
		Machine Model (MM)	±200	V

ESD (electrostatic discharge) sensitive device
Live devices and circuit boards can be electrically charged without being noticed. Although this product has a patented or proprietary protection circuit, the device may be damaged in the event of high energy ESD. Therefore, appropriate ESD preventive measures should be taken to avoid device performance degradation or function loss.

Recommended Operating Conditions (1)

Table 7.1

Parameter		MIN	MAX	UNIT
VIN	VCC/VCCP-GND	4.5	5.5	V
	EN-GND	2	5.5	
	VIN-GND	4.5	24	
VOUT	V_{OUT}	0.65	2	
I_{OUT}	I_{OUT}	0	28	A

(1) The recommended working conditions are designed to make IC work normally, but do not guarantee the performance of specific parameters. For details, please refer to the technical specifications in the following article.

Technical Specifications

Unless otherwise specified, VCC=VCCP=5V，VOUT=1V，T_A=25℃. Maximum min applies to -40℃<T_A=T_J<125℃

Table 8.1

Parameter		Test Conditions	MIN	TYE	MAX	UNIT
Input						
VCC	VCC Operation Voltage		4.5	5	5.5	V
VCCP	VCCP Operation Voltage		4.5	5	5.5	V
V_{CC_TH}	VCC Threshold Voltage	Rising	4.1	4.3	4.5	V
V_{CC_UVLO}		Falling	3.5	3.9	4.1	V
V_{CCP_TH}	VCCP Threshold Voltage	Rising	4.0	4.3	4.5	V
V_{CCP_UVLO}		Falling	3.5	3.9	4.1	V
I_{Q_VCC}	VCC Quiescent Current	VID0=VID1=0V, EN=5V		300	600	μA
I_{SD_VCC}	VCC Shutdown Supply Current	EN=0V		5		μA
I_{BST_L}	BST bias current	V_{BST} = 34 V, V_{SW} = 28 V, T_A = 25°C		0.1	1	μA
I_{SD_BST}	BST Shutdown Supply Current	EN=0V, BST=5V, SW=0V, T_A = 25°C			1	μA
ENABLE						
V_{EN_R}	Enable voltage threshold	Rising	1.52			V
V_{EN_F}		Falling			0.55	V
I_{EN_B}	EN Input Bias Current	EN=5V			1	μA
V_{EN_MAX}	EN Maximum input voltage			5.5	6	V
2-Bits VID						
V_{VID_H}	VID High Threshold Voltage		1.52			V
V_{VID_L}	VID Low Threshold Voltage				0.55	V
I_{VID_L}	VID Leakage Current	VID=0V			100	nA
I_{VID_L}	VID Input Bias Current				1	μA
T_{VID_D}	VID Delay time (1)	Any VID edge to 10% of FB change		200		us
PG Indication						
V_{PG_L}	Power Good High Leakage Current	$I_{PG\ (sink)}$=4mA		52	80	mV
I_{PG_HL}	PG sets high leakage current				200	nA
R_{PG_L}	PG pull-down conduction resistor			13		Ω
T_{PG_D} (1)	Power Good Startup Delay	Measure from SSEND to PG pos edge		3.8		ms
T_{PG_H}	Power Good Propagation Delay	Delay for power good in		3.4		ms
T_{PG_L}		Delay for power good out		0.35		ms
$T_{MASKING}$	Power Good Masking Time	Triggered by any VID Change		425		us
Power Stage						
$F_{SW\_Accuracy}$	Switching frequency accuracy				±10	%
F_{SW}	Switching frequency	R_{FSET}=2K		300		KHZ
		R_{FSET}=6K		400		
		R_{FSET}=10K		600		
V_{DET}	Frequency Detection	F_{SW}=300K			220	mV

	voltage threshold	F_{SW}=400K			350	mV
		F_{SW}=600K	450			mV
R_{SW_L}	SW pull-down resistance		85			kΩ
R_{GHH}	GH Pull−High Resistance	I_{BST-GH} = 100mA		0.7	1.2	Ω
R_{GHL}	GH Pull−Low Resistance	I_{GH-SWN} = 100mA		0.5	0.8	
R_{GLH}	GL Pull−High Resistance	$I_{PVDD-GL}$ = 100mA		0.7	1.2	
R_{GLL}	GL Pull−Low Resistance	$I_{GL-PGND}$ = 100mA		0.5	0.7	
I_{GH_Source}	GH Source Current (1)			2		A
I_{GH_SINK}	GH Sink Current (1)			2		A
I_{GL_Source}	GL Source Current (1)			2		A
I_{GL_SINK}	GL Sink Current (1)			4		A
I_{DET}	Frequency detection current			50		μA
T_{DET}	Oscillator frequency detection time			200		us
T_{SD}	Dead Time	GH off to GL on		20		ns
		GL off to GH on		20		
T_{ON_MIN}	Minimum MOS conduction time on high side (1)			35		ns
T_{OFF_MIN}	Minimum MOS turn-off time on low side (1)			250		ns
Internal BST Diode						
V_{DIODE}	Schottky diode voltage drop	I_F = 1mA, T_A = 25°C		0.3		V
		I_F = 10mA, T_A = 25°C		0.5		V
Error Amplifier						
Error amplifier dc gain (1)			80			dB
Error amplifier open-loop bandwidth (1)				20		MHz
FB bias voltage (1)		Relative to CSN = VID	-1		1	uA
Slew Rate (1)		COMP pin to GND = 10 pF		10		V/us
Maximum output voltage (1)		10 mV of overdrive, I_{SOURCE} = 2.0 mA		VCC		
Minimum output voltage (1)				0.2	0.3	V
Output Source Current		10 mV of overdrive, VOUT= 0.3 V	2			mA
Output Sink Current		10 mV of overdrive, VOUT=1V	2			mA
Soft Start						
I_{CHG-SS}	VREF soft start charging current			20		μA
$I_{CHG-VID}$	VREF increases the charging current	VREF 0.65V-2V		80		
$I_{DISC-VID}$	VREF decreases the discharge current	VREF 2V-0.65V		80		
Soft Stop						
R_{DISC}	Output relief resistance (via SCN)			24		Ω
Feedback Voltage						
I_{FB}	FB leakage current		-500		500	nA
V_{FB}	FB voltage range		0		2	V
V_{FB_OV}	FB overvoltage threshold (1)			2		V
$V_{FB\_TH\_OV}$	V_{FB_OV}-VID SET (2)	Relative to nominal VID Voltage	200	300	400	mV
$V_{FB\_TH\_UV}$	V_{FB_UV}-VID SET (2)		-250	-200	-150	mV
T_{FB_UV}	FB Undervoltage determination time			3		μs

$V_{FB\_Accuracy}$	Accuracy of feedback voltage		-1		1	%
		T_A=25℃	-0.35		0.35	%
V_{REF}	Internal reference voltage			0.65		V
T_{FB_OV}	FB Over Voltage Delay			2		μs
Differential Current Sense Amplifier						
CSP-CSN common mode input voltage range		Reference ground is AGND	-0.2		2	V
Differential input voltage range			-30		30	mV
Over Current Protection (OCP)						
OCP Threshold		V_{SCP}-V_{CSN}	25	30	35	mV
LOADLINE						
LOADLINE Signal amplification factor		(V_{VDRP}-V_{VREF})/(V_{CSP}-V_{CSN})		6		
Thermal Shutdown						
T_{SD}	Thermal shutdown (1)			150		℃
T_{SD_H}	Thermal shutdown delays (1)			25		℃

(1) Guaranteed by characterization or design, not production tested

(2) Test results at V_{REF}=0.65V

Functional Block Diagram

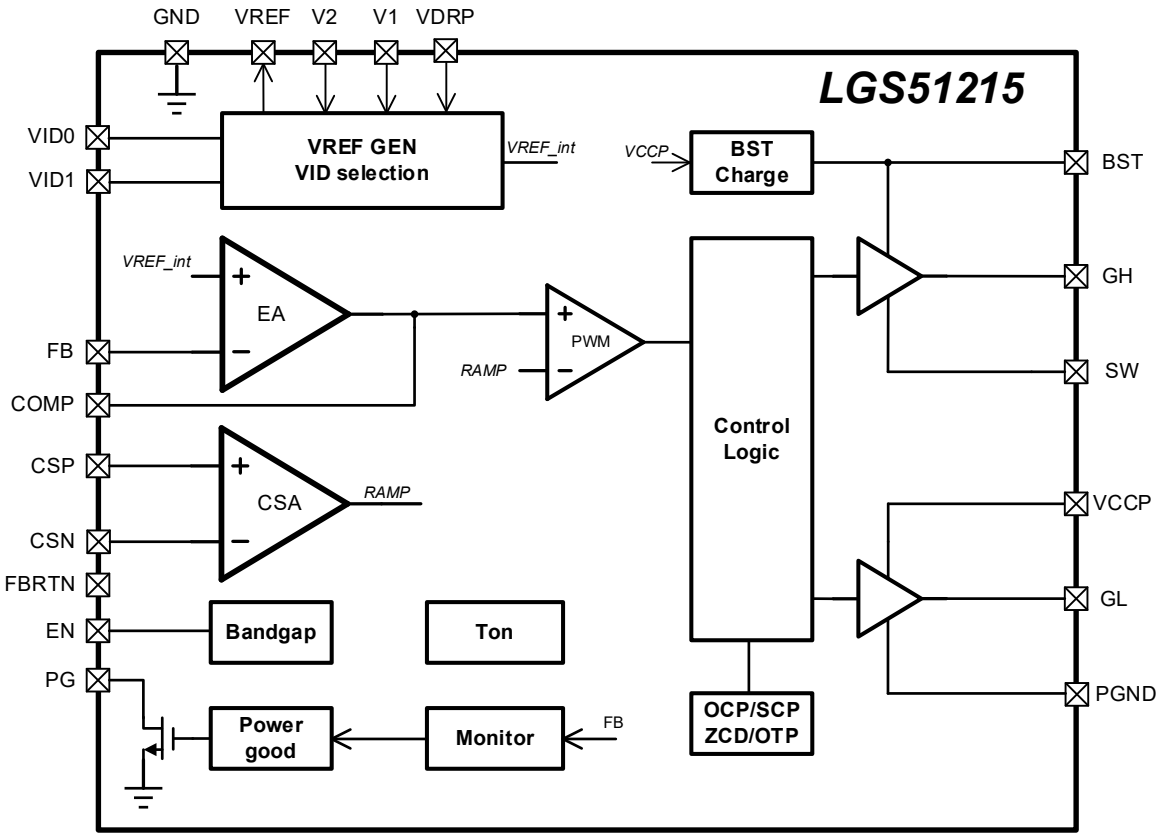


Figure 9.1 Internal function block diagram

Typical Application Recommendation

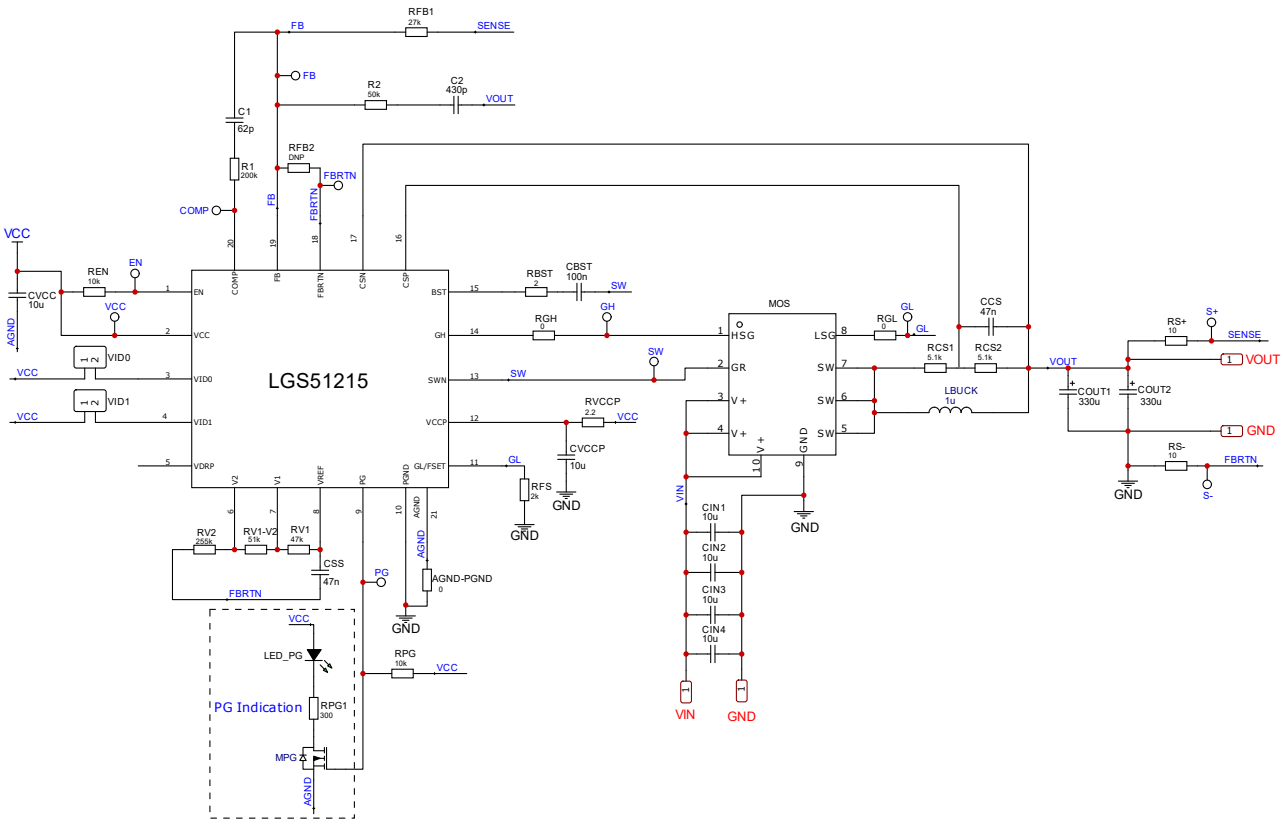


Figure 10.1 Application Circuit Recommendation (VIN=4.5-24V(typical value 12V), VOUT=1V，IO_{MAX}=30A，Fsw=300kHz)

Table 10.1 LGS51215 Typical external devices are recommended

Designator	QTY	Description	Manufacturer	Part Number
MOS	1	30V Asymmetric Dual N-Channel MOSFET	ON Semiconductor	FDPC5018SG
CIN1-4	4	10μF, 50V, X5R, 1210, ceramic	SANYEAR	C1210X7R106M500NT
COUT1-2	2	220μF, 2.5V, 7343, 9 mill-ohm ESR	PANASONIC	2R5TPE220M9
LBUCK	1	1μH, ±20%, 1040, 2.3mΩ DCR	KEMET	MPCH1040L1R0
		2.2μH, ±20%, 1040, 3.43mΩ DCR	VISHAY	IHLP-5050FD-51

(1) It is recommended to use X7R or X5R ceramic capacitors for power input and place them as close to IC as possible. See the following description of recommended input capacitors.

(2) For capacitors from BST to SW and VCCP to GND, please select ceramic capacitors with voltage resistance higher than 10V and place them as close to IC pins as possible.

Typical Characteristics

Unless otherwise specified, VIN=12V，VOUT=1V，T_A=25℃

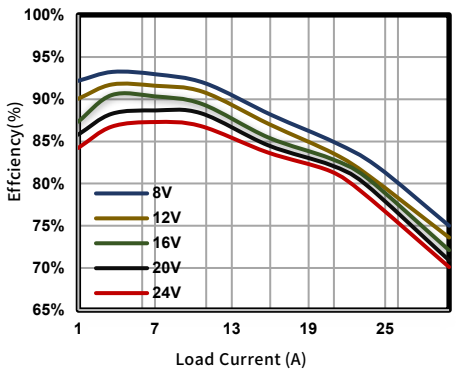


Figure 11.1 Efficiency vs Load Current for VOUT=1V

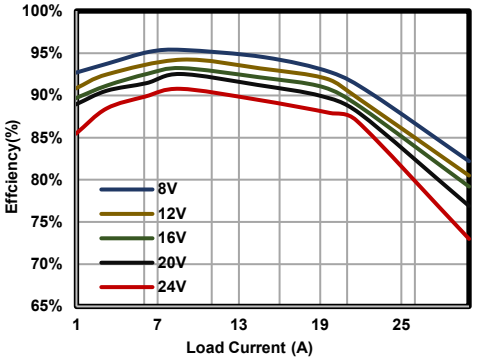


Figure 11.2 Efficiency vs Load Current for VOUT=1.8V

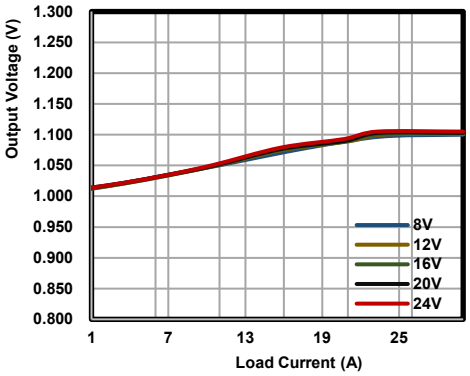


Figure 11.3 VOUT=1V vs Load Current with Load line

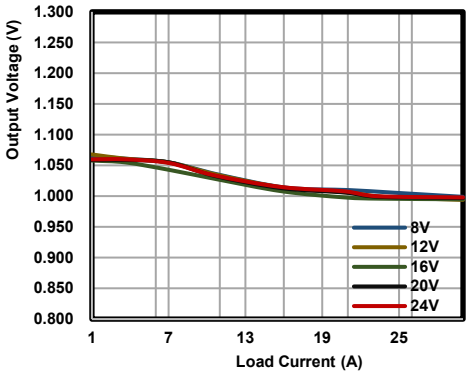


Figure 11.4 VOUT=1V vs Load Current

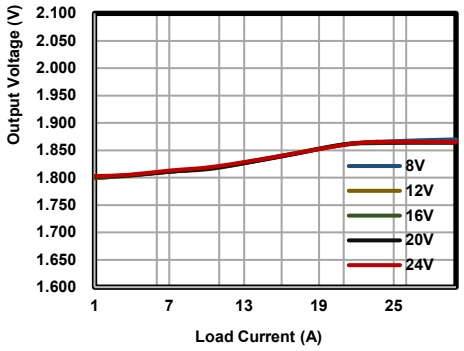


Figure 11.5 VOUT=1.8V vs Load Current with Load line

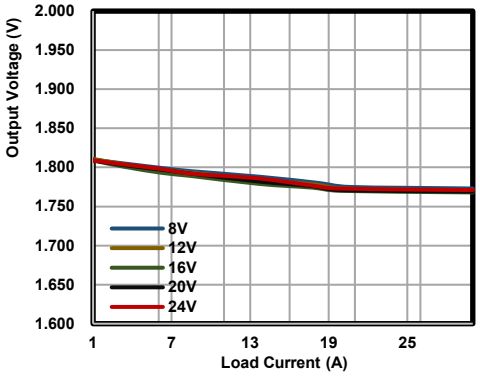


Figure 11.6 VOUT=1.8V vs Load Current

LGS51215

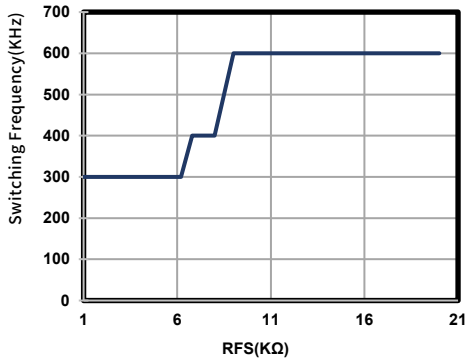


Figure 11.7 R_{FS} vs Switching Frequency

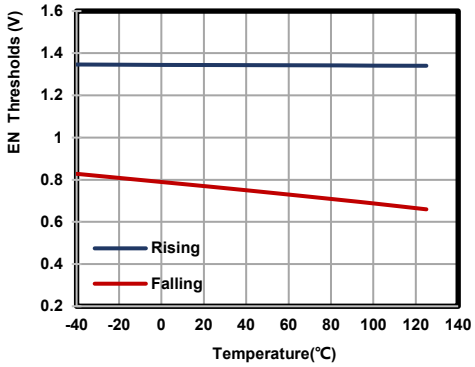


Figure 11.8 EN Thresholds vs Temperature

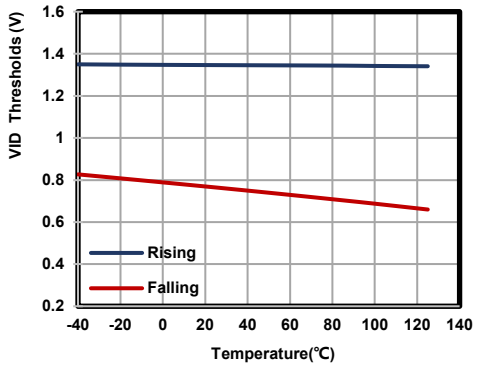


Figure 11.9 VID Thresholds vs Temperature

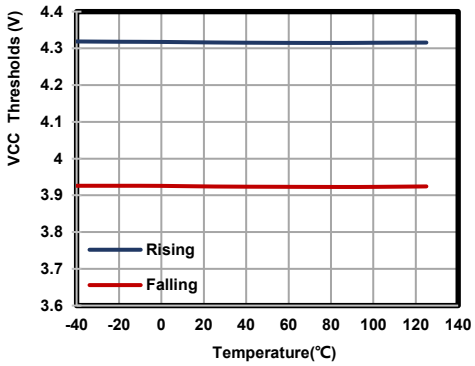


Figure 11.10 VCC Thresholds vs Temperature

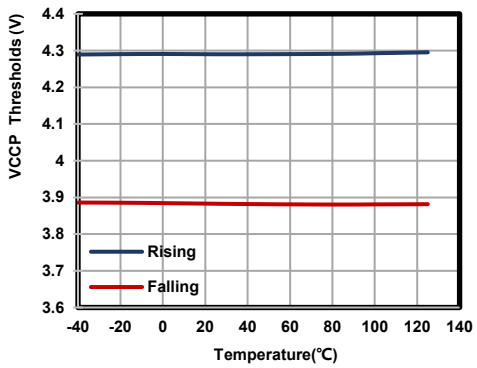


Figure 11.11 VCCP Thresholds vs Temperature

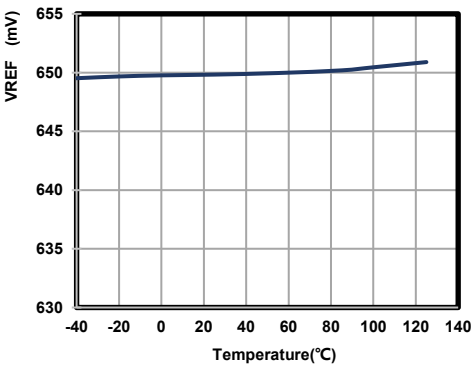


Figure 11.12 V_{REF} vs Temperature

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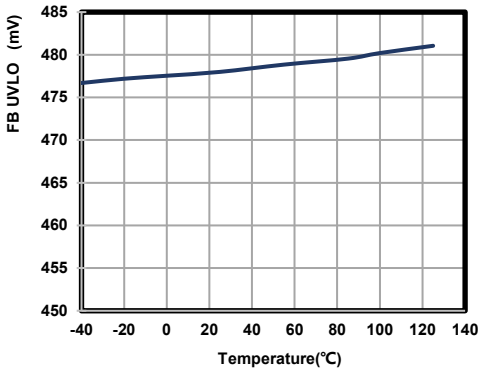


Figure 11.13 FB UVLO vs Temperature

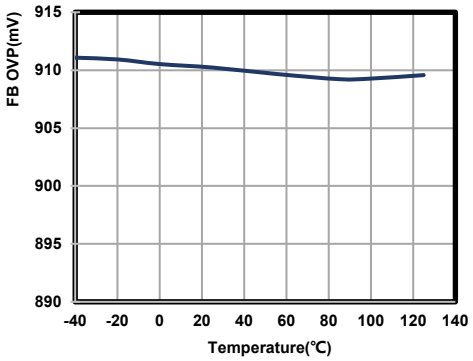


Figure 11.14 FB OVP vs Temperature

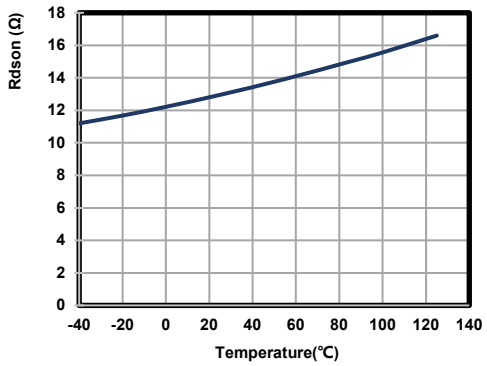


Figure 11.15 PG Open-drain Rdson vs Temperature

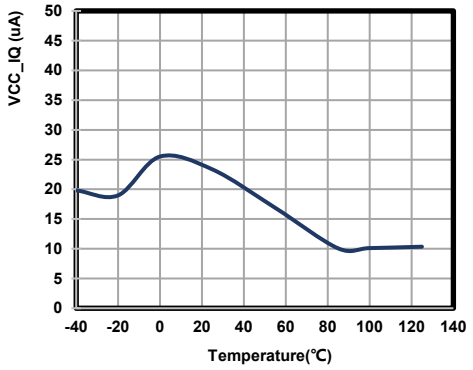


Figure 11.16 VCC_IQ vs Temperature

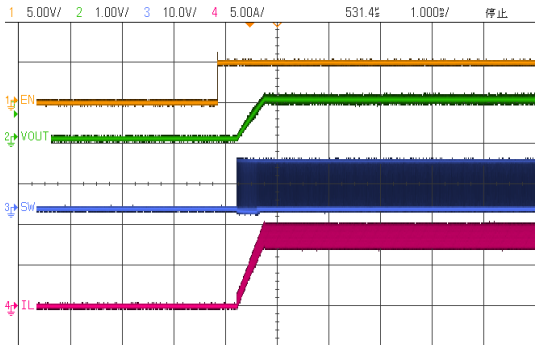


Figure 11.17 EN Power On (1)

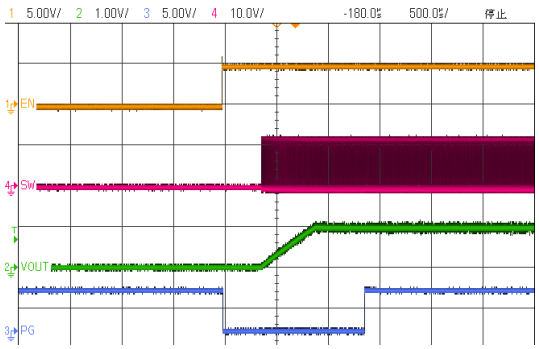


Figure 11.18 EN Power On (2)

LGS51215

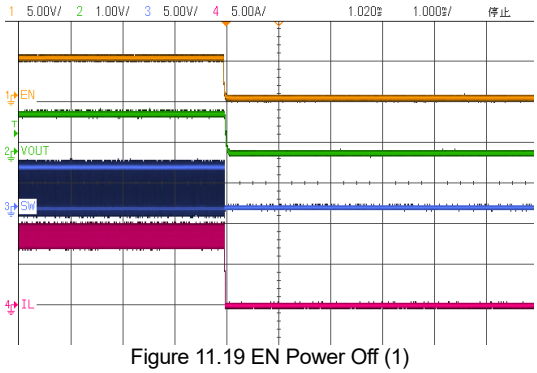


Figure 11.19 EN Power Off (1)

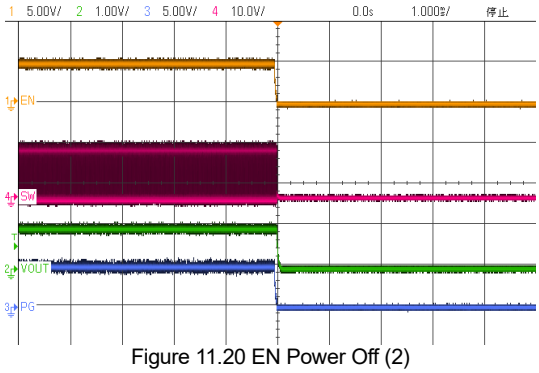


Figure 11.20 EN Power Off (2)

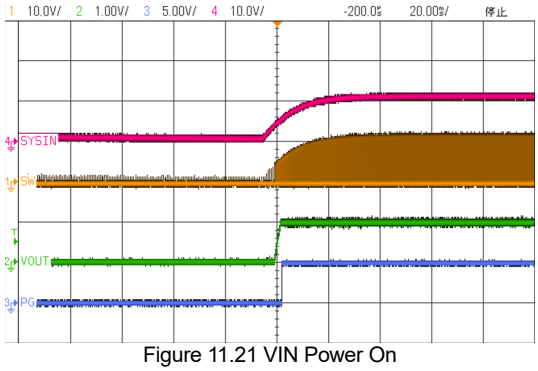


Figure 11.21 VIN Power On

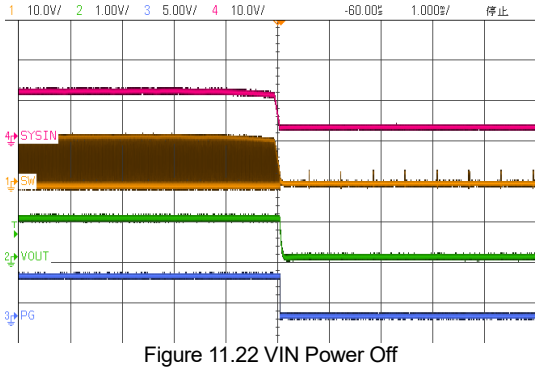


Figure 11.22 VIN Power Off

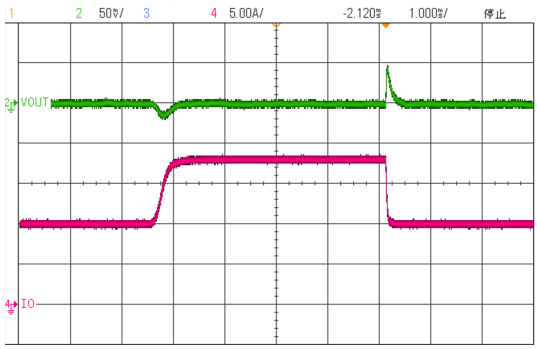


Figure 11.23 Load Transient 10-18A

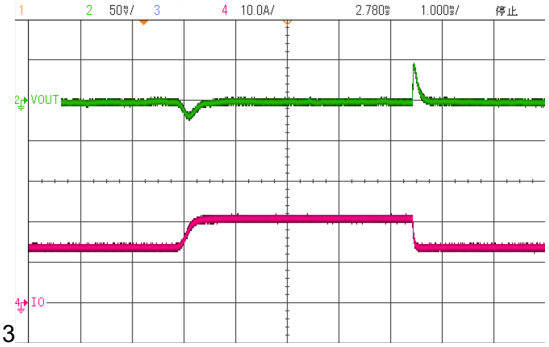


Figure 11.24 Load Transient 14-22A

LGS51215

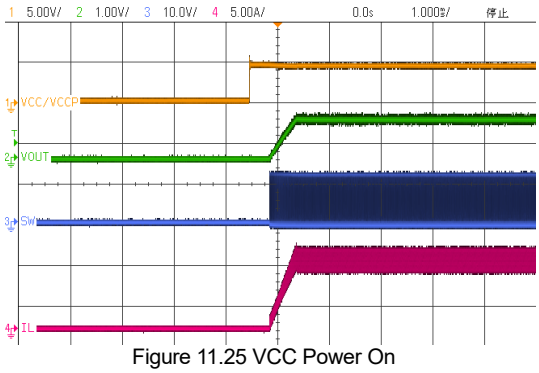


Figure 11.25 VCC Power On

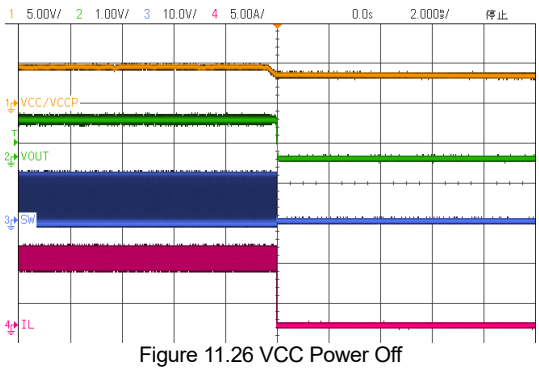


Figure 11.26 VCC Power Off

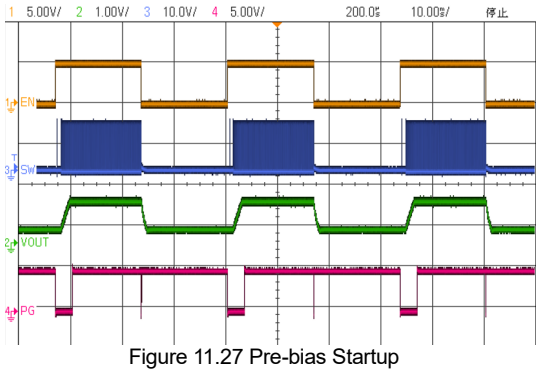


Figure 11.27 Pre-bias Startup

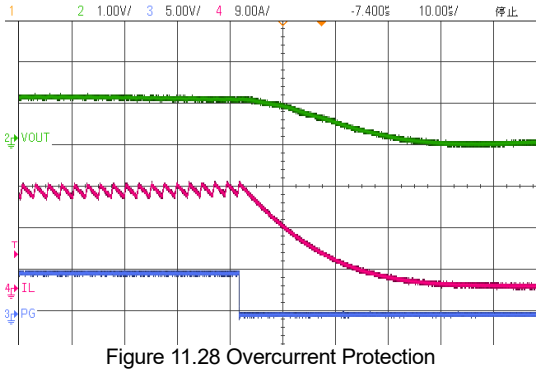


Figure 11.28 Overcurrent Protection

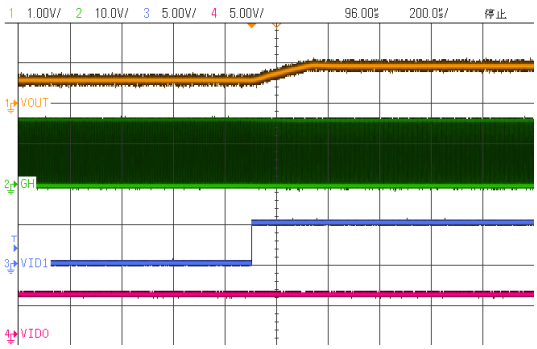


Figure 11.29 VID Change 0.65V-1V

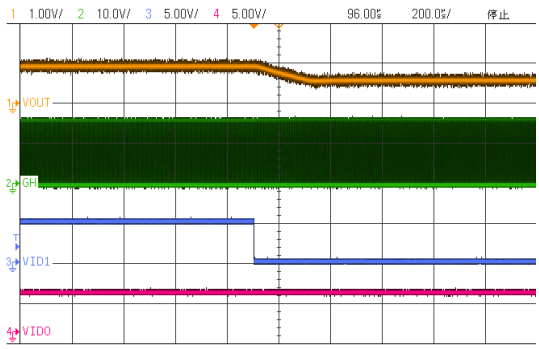


Figure 11.30 VID Change 1V-0.65V

Application Information

Overview

LGS51215 synchronous buck controller can operate in the 4.5V to 24V input voltage (VIN) range, providing a natural transition between PFM and CCM, maintaining high efficiency and stability under light load while supporting fast transient response. LGS51215 provides the control functions and protection circuits necessary for a general-purpose controller to meet a wide range of application requirements. LGS51215 supports the output voltage setting function and has a 2-bit VID control mode, which can dynamically change the output voltage of four gears (including 0V) and its switching rate. LGS51215 requires an external 5V voltage source to power and control the internal circuit. The under-voltage locking (UVLO) function protects the internal circuit from low input voltages. LGS51215 can be configured with external resistors to switch frequencies around the 300KHz,400KHz, and 600KHz three-step frequency ranges. LGS51215 provides an upper and lower power tube drive circuit with adaptive dead time, changeable soft start time and extremely low turn-off current, as well as over current protection, good output status monitoring, over voltage protection, under voltage protection, built-in output discharge circuit and thermal turn-off.

Reference Voltage Programming

LGS51215 provides 2-bit VID control, with four VREF reference voltages (relative to FBRTN) selected by changing the VID state. The design will allow the output voltage to be as low as 0.65V (the internal reference voltage value). When VID0 and VID1 are both low, LGS51215 will turn off GH and GL (the upper and lower power tube drive function). The output voltage will decay gradually to 0V through load consumption.

The VID truth tables for each part are listed below.

Table 12.1 VID Truth Table

VID State		Results		
VID1	**VID0**	**Close**	**VREF(V)**	**VOUT(V)**
0	0	\	0	0
0	1	S0	V_{REF0}	VOUT1
1	0	S1	V_{REF1}	VOUT2
1	1	S2	V_{REF2}	VOUT3

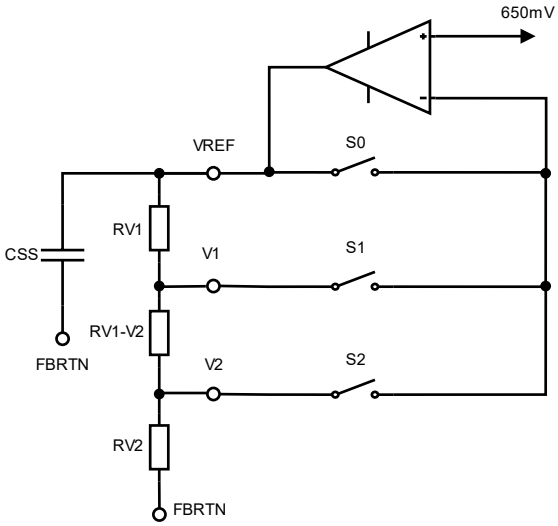


Figure 12.1 External Reference Voltage Setting

As the picture above shows, When VREF≠0, VREF can be calculated based on the following equations:

$$V_{REF0} = V_{REF-IN} = 650\text{mV}$$

$$V_{REF1} = V_{REF0} \cdot \left(1 + \frac{R_{V1}}{R_{V1-V2} + R_{V2}}\right)$$

$$V_{REF2} = V_{REF0} \cdot \left(1 + \frac{R_{V1} + R_{V1-V2}}{R_{V2}}\right)$$

Note: $V_{REF2} > V_{REF1} > V_{REF0}$. To ensure system stability, keep the total resistance from VREF to FBRTN greater than 100K.

Output Voltage VOUT Setting

Adding a resistor RFB2 from the FB pin to the FBRTN to form a feedback voltage divider with the resistor RFB1 can be used to increase the output voltage. If the resistor RFB2 is left vacant, the output voltage VOUT will be equal to the voltage of FB. The design keeps the output voltage setting entirely dependent on user requirements, making the LGS51215 more flexible to use.

As shown in Figure 12.2, output voltage can be calculated based on the following equations:

$$VOUT1 = V_{REF0} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

$$VOUT2 = V_{REF1} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

$$VOUT3 = V_{REF2} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

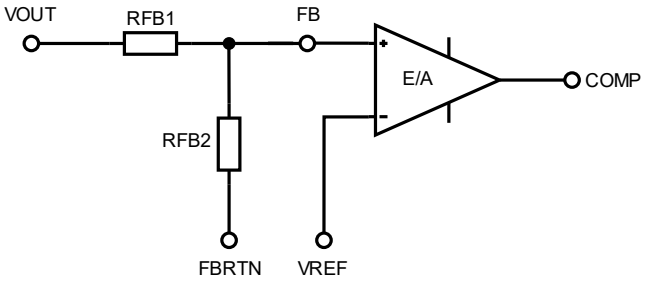


Figure 12.2 Feedback voltage divider

Differential Sensing of Output Voltage

LGS51215 output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point. FBRTN should be connected directly to the negative remote sensing point. The LGS51215 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to provide accurate output voltage.

External Soft−Start Setting and VID Change Slew Rate

To limit the start−up inrush current, a capacitor can be connected from VREF pin to ground to ramp up reference voltage slowly. During this period, the set amplifier output 20 μA current to charge capacitor C_{SS}. When the VREF voltage is less than the set value, the VREF voltage value follows the soft starting voltage, and will no longer rise when the VREF voltage reaches the set value. In this process, the soft starting voltage continues to rise until the capacitor is charged.

The output current of the set amplifier will change to +83μA/−80μA after soft start period. So during voltage steps due to VID bit change, the slew rate of output voltage. To ensure the stability of the loop operation, please use a high tolerance type MLCC, such as X7R.

Adaptive Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET free-wheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. LGS51215 implements adaptive dead time control to minimize the dead time, as well as preventing shoot through from happening.

Soft Stop

LGS51215 has Soft Stop discharge mode. a fault (UVP, OVP, OCP, TSD) or disable (EN) causes the output to be discharged through an internal 24−ohm transistor inside of the CSN Pin. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

Switching Frequency and detection

LGS51215 switch frequency range is set by the resistor R_{FS} on the GL/FSET pins. After LGS51215 is enabled, the detection switch frequency is set before soft startup. The GL/FSET pin provides 50μA detection current I_{FDECT}. After 200μs detection time, the voltage of GL/FSET pin is measured to determine the frequency detection threshold. It should be noted that I_{FDECT} takes longer to charge the GL/FSET pins when the gate capacitance of the low-side MOSFET exceeds 10nF, so users should consider the voltage rise time of GL/FSET during use to ensure that the detection process is completed within 200μs. You can directly use the MOSFET listed in the recommended list of LGS51215 peripherals to ensure the normal use of the chip.

Resistor selection for frequency configuration, please refer to the following table:

Value Of R_{FS}	2K	6K	10K

F_{SW}	300KHz	400KHz	600KHz

Power Save Mode

If the load current decreases, LGS51215 will enter power save mode operation. During this mode, the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintains high efficiency. The Skip Comparator manages and switches CCM and PFM by comparing the built-in I_{SKIP} and I_{REF}. When the current demand is lower than I_{SKIP}, the comparator controls the suspension of switching. When the current demand increases (VOUT drops), the comparator controls the activation of the current loop into CCM mode, making VOUT rise, at which time the I_{REF} will drop, when the I_{REF} is lower than I_{SKIP}, the switching power tube again suspends switching.

The output voltage ripple in this mode is larger than that in CCM mode because the output voltage drops and recovers irregularly.

EN——IC Enabled

The EN voltage controls the startup and shutdown of LGS51215. When the EN voltage is less than V_{EN_OUT}, the chip remains in low-power standby state. When the voltage at the EN pin is higher than V_{EN_OUT}, the IC enters soft start mode. During IC shutdown, when EN pin voltage drops to V_{EN_OUT} - V_{EN_HYST}, LGS51215 regulator stops working and re-enters standby.

During the test, EN pin can be connected to the VCC through a 10KΩ resistor, which can be kept on when the VCC is powered on. In actual applications, users can flexibly enable EN based on the application environment.

Note: EN pin has a maximum voltage withstand of 6V and a rated operating voltage of 5V.

Under Voltage Lockout

There is under-voltage lockout protection for VCC in LGS51215, which has a typical trip threshold voltage 4.3V and trip hysteresis 400 mV. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. This protection does not trigger a fault timer to put the chip into the Shutdown state.

Over Voltage Protection and Under Voltage Protection

When FB voltage is 300 mV (typical) above VREF voltage for over 2 μs blanking time, an OV fault is set. At that moment, the top gate driver is turned off and the bottom gate driver is turned on trying to discharge the output. The bottom gate driver will be turned off when V_{FB} drops below under voltage threshold. EN resets or power recycle the device can exit the fault.

The under-voltage limit is 300 mV (typical) below VREF voltage. If V_{FB} is below this threshold over 3.3 μs, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault.

Note: UVP is delayed for soft start after EN goes high. UVP is disabled during VID changes and when VOUT = 0V.

Power Good Monitor

LGS51215 provides window comparator to monitor the FB voltage. The PG pin is open drain 5−mA pull down output that needs to be connected to the VCC using a pull-up resistor. During startup, PG stays low until the feedback voltage is within the specified range for about 3.3 ms.

Note:
(1) The power−good circuit is masked during any VID change. The duration of the PG mask is set to approximately 425μs by an internal timer.
(2) PG pin cannot be pulled to a voltage higher than VCC pin voltage.

Over Current Protection (OCP)

LGS51215 continuously monitors the current flowing through the inductor through differential current detection. The current limiting threshold ΔV_{TH} is 30mV. When the inductor current exceeds the current limiting threshold, the high-side power tube driver (GH) will be turned off periodically.

During the operation of the module, the inductance DCR may be deviated due to the influence of temperature drift. An NTC resistor can be added at RCS2 to compensate for temperature.

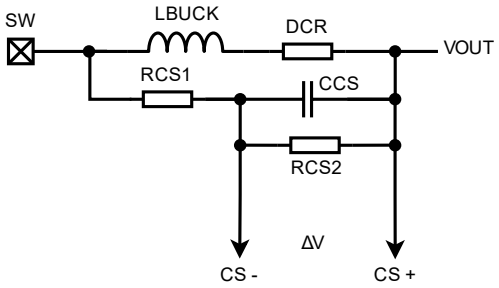


Figure 12.3 Inductive DCR current detection circuit

As shown, the inductance current limit can be configured by resistors RCS1, RCS2 and the DCR of the inductor:

$$I_{LIM} = \frac{\Delta V}{DCR} \cdot (1 + \frac{RCS1}{RCS2})$$

Loadline

LGS51215 allows user to program loadline via the VDRP pin. As illustrated in Figure 12.4, LGS51215 outputs a differential signal between VDRP and VREF pins, with its amplitude six times as that of differential signal across CSP and CSN pins. Consequently, user can program a loadline with a resistor, RDRP, between VDRP pin and FB pin, as shown in the following equation:

$$Loadline = 6\Delta V \cdot \frac{RFB1}{RDRP} + VREF$$

If this feature is not required, keep the VDRP pins empty.

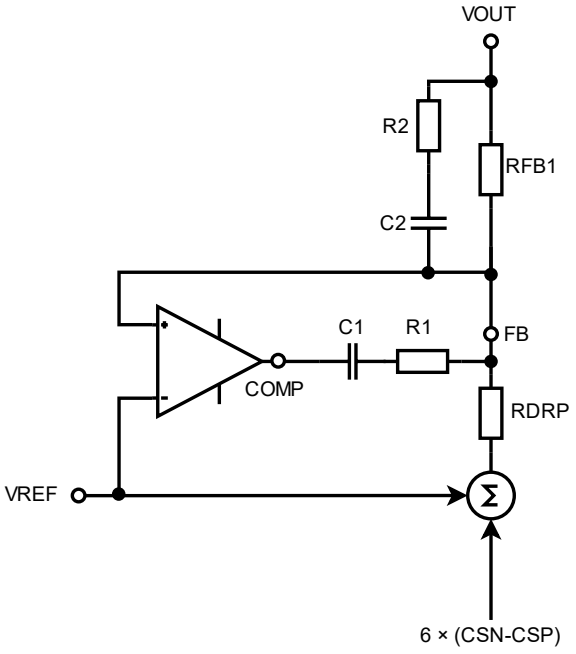


Figure 12.4 Load line Circuit

Pre−Bias Startup

In some applications, the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. LGS51215 supports pre−bias start up. When the load is started with pressure, the output voltage can be monotonously increased and the back current can be avoided.

Thermal Shutdown

When the junction temperature rises above 150℃, Thermal Shutdown is activated and the system pulls the COMP pin voltage to GND to Shutdown the upper and lower MOSFET. When the junction temperature drops below 130℃, LGS51215 automatically restarts using the soft start function.

The guaranteed operating junction temperature range of the device is -40℃ to +125℃, high junction temperature will reduce the working life, when the junction temperature is higher than 125℃ for a long time, the device life will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on the specific operating conditions as well as the PCB layout, package thermal rating, and other environmental factors.

Junction temperature (T_J, unit: ℃) is calculated according to the ambient temperature (T_A, unit: ℃) and power (P_D, unit: W). The calculation formula is as follows:

$$\boldsymbol{T_J = T_A + (P_D \times \theta_{JA})}$$

Note：θ_{JA} (unit: ℃/W) is thermal resistance of packaging.

PCB Layout and Cabling Guide

Proper PCB layout is critical for the high current, fast switching circuit (with high current and high voltage slew rate) module where LGS51215 controller resides to ensure proper operation and stable output of the buck module. Poor layout can affect the performance of LGS51215, resulting in current sampling deviation, electromagnetic interference, poor electromagnetic compatibility and voltage loss, which in turn affects the stability of use.

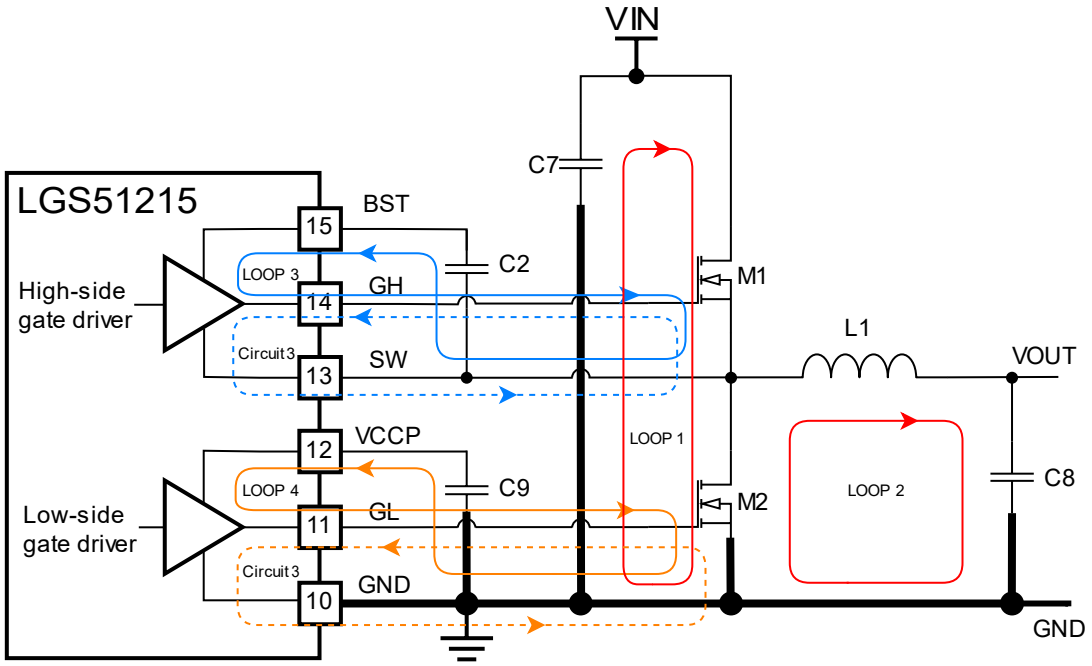


Figure 13.1 Power circuit

Power Stage Layout

VIN input capacitance, output capacitance, and high and low side MOSFET are the power-level parts of the BUCK topology and are typically placed on top of the PCB to maximize convection heat dissipation. Small-signal components can be placed on the back, and at least one internal electrical layer directly connected to GND is added between the top and bottom layers to shield and isolate small signals and noise.

- Loop 1 is the main switching loop circuit of the power stage. The topology of the buck converter determines that a particularly high di/dt current flows through it. Therefore, the loop area of this part must be minimized to minimize parasitic inductance, and the input capacitance of VIN must be kept as close as possible to the drain of the high-side MOSFET. Loop 2 is a loop from the low-side MOSFET through the GND terminal of the inductor and the output capacitor back to the source of the low-side MOSFET. Connect the source of the low-side MOSFET and the negative terminal of the output capacitor as close to GND as possible. Although the current flowing through the inductor and the VOUT output capacitor will be limited by the inductor, the area of Loop 2 should also be designed to be as small as possible.
- The SW pin serves as the switch node of the BUCK module, connecting the source pole of the high side MOSFET, the drain pole of the low side MOSFET, and the high voltage side of the inductor. The design area of the SW pin as an interference source on the PCB should not be too large. This part of the design can be considered according to the layout provided by the MOSFET manufacturer. The high-frequency ringing generated by the resonant loop consisting of the output capacitor and the parasitic inductor generated by the power tube is directly reflected on the SW node

and the peak voltage of the ringing, if not controlled, may exceed the value of the input voltage. To ensure that the peak value of the ringing does not exceed the absolute maximum voltage value of the SW pin, a resistor with a low resistance value (generally 1-3Ω) can be added to the driver or a buffer consisting of resistors and capacitors can be connected in series between the SW node and GND to reduce the peak value of the ringing.

Gate Drive Layout

LGS51215's high and low side gate drives include short control delays and adaptive dead zone times, and are capable of responding quickly to rapid ups and downs of high currents, which can cause unacceptable ringing if the PCB is poorly designed. The key to optimize the grid drive is to reduce the parasitic inductance of the circuit, including the series resonant inductance and common source inductance of the grid.

- Loop 3 is the driving circuit of the high-side MOSFET. When the high-side MOSFET is on, the high current flows from the bootstrap capacitor of the BST pin (C2 in Figure 13.1) through the gate drive of the high-side MOSFET, and returns to the negative electrode of capacitor C2 through the SW node. On the contrary, when the high-side MOSFET is closed in loop 3 (the dotted line loop in Figure 13.1 is the same as loop 3), the high current flows from the gate of the high-side MOSFET through SW to return to the source of the high-side MOSFET. Loop 4 is the low side MOSFET drive loop. When the low side MOSFET is on, the large current flows from the capacitor (C9 in Figure 13.1) of VCCP pin to the ground through the gate drive of the low side MOSFET and returns to the negative pole of capacitor C9 via GND. On the contrary, when the low side MOSFET is closed in loop 4 (the dotted line loop with the same color as loop 4 in Figure 13.1), the large current flows from the gate of the low side MOSFET through GND back to the source of the low side MOSFET.
- The gate path from gate driver GH、 GL to high and low side MOSFET should be as short as possible to reduce series parasitic inductance, and use 25mil or wider wiring as far as possible.
- Capacitor C2 should be close to BST and SW pins to minimize loop area of high-side MOSFET drive; The capacitor C9 should be close to the VCCP and GND pins to minimize the loop area of the low-side MOSFET drive.
- Add a resistance of 2Ω-10Ω next to the capacitor C2 of loop 3 to slow down the opening speed of the high side MOSFET, thus reducing the peak ringing value of the SW node at the expense of the switching loss of the high side MOSFET.

Controller Layout

The PCB layout of analog signal, feedback signal and current limiting circuit of the whole step-down module LGS51215 should be considered very carefully:

- A ground plane is generally required to separate the power level from the signal layer to provide good noise shielding.
- All sensitive analog signals and components (such as COMP,FB, CSN, CSP) should be kept away from high voltage switching nodes (SW, GH, GL, BST) to avoid coupling.
- The feedback resistor R8 can be directly connected to the output voltage VOUT detection point or to the output large capacitor.
- Differential detection of CSN and CSP needs to be side by side on the same PCB layer or overlapping on adjacent layers. The OCP setup resistor R9 is connected between the CSP and VOUT. Ensure that the resistor is as close to the LGS51215 controller as possible to avoid coupling of the connection loop from CSP to R9 with the high voltage node.
- The current loop of VCC, VCCP and VIN to GND through their respective decoupling capacitors is minimized, even if these decoupling capacitors are placed as close to the IC as possible.

Thermal Layout

For a switching power supply controller like LGS51215, the operating temperature range is influenced by many factors, such as the average gate drive current of a power MOSFET, switching frequency, input voltage, package characteristics, and operating environment.

- In order for LGS51215 to work stably within the specified temperature range, the package must be able to dissipate heat effectively while keeping the junction temperature within the rated range. LGS51215 uses a 3mm x 3mm QFN-20L package that provides a heat dissipation PAD at the bottom to effectively remove heat in the package. The PCB design should be equipped with heat shield, heat dissipation through hole, and grounding plane to assist the heat dissipation PAD to complete heat dissipation.

- The drain of the high MOSFET is connected to the VIN plane for heat dissipation, while the drain of the low MOSFET is connected to the SW plane, but the SW area is deliberately designed to be relatively small compared to the VIN plane to alleviate electromagnetic interference problems.

PCB Layout Reference

Figure 14.1 provides a reference PCB layout for LGS51215 applications. For more information about recommended application solutions, refer to the LGS51215 EVM Board user manual.

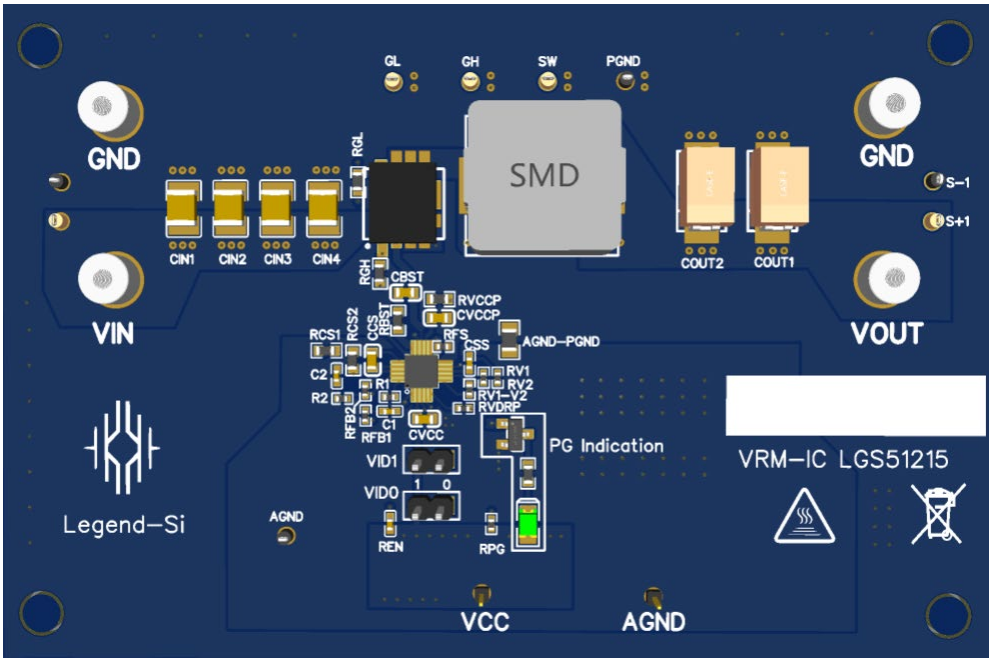
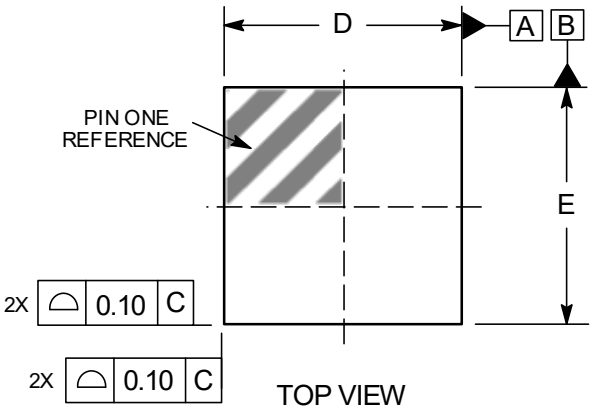
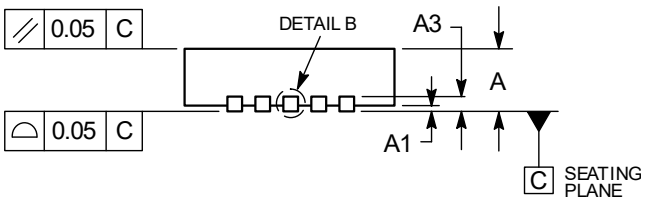


Figure 14.1 PCB Layout Reference

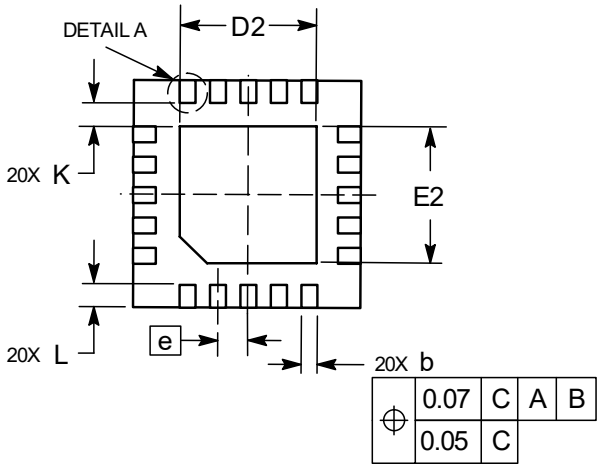
Description Of Package



TOP VIEW



SIDE VIEW



BOTTOM VIEW

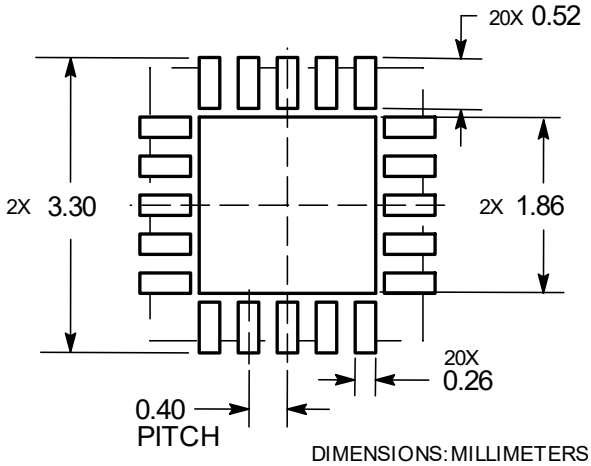
DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.40 BSC	
K	0.20 REF	
L	0.20	0.40

NOTE:

(1) All linear dimensions are in millimeters. Any dimensions in parentheses are for reference only. Dimensioning and tolerancing per ASME Y14.5M

(2) This drawing is subject to change without notice.

(3) This dimension does not include the burrs of the moulds. The burrs or protrusions on each side of the moulds shall not exceed 0.25 mm.



SOLDERING FOOTPRINT

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